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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,020	10/21/2003	Philip Neaves	501317.02 (30302/US)	4992

7590 06/10/2005

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EXAMINER	
NGUYEN, TUNG X	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/691,020	NEAVES ET AL.
	Examiner	Art Unit
	Tung X. Nguyen	2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-32 and 44-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-32 and 44-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/04, 4/05, 5/04,*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of species IV with claims 25-32, and 44-47 in the reply filed on 5/24/05 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 25, 27, 29, 30, 32, 44, 46-47 are rejected under 35 U.S.C. 102(b) as being anticipated by Cilingiroglu (u.s.p 5,124,660).

As to claims 25, 30, Cilingiroglu disclose in Figs. 1-5, a method for evaluating an integrated circuit (110 of figure 1) having a plurality of data terminals (112 of figure 1) at which data signals are received, the method comprising: capacitively coupling a test plate (106 of figure 1) to a plurality of signal terminals (112 of figure 1) at which data signals are received; transmitting a data signal from the test plate to one of the plurality of signal terminals (col. 3, lines 31-47); and evaluating the data signal detected by at the signal terminal against a test criteria (col. 3, lines 31-47).

As to claim 27, Cilingiroglu disclose in Figs. 1-5, ceasing reception of the data signal from the first signal terminal (via 516 of figure 5); transmitting a data signal from the test plate to another one of the plurality of signal terminals (via 516 of figure 5); and

evaluating the data signal detected by other signal terminal against the test criteria (col. 5, lines 30-40).

As to claim 29, Cilingiroglu disclose in Figs. 1-5, decoupling the test plate (106 of figure 1, 502-504 of figure 5) from a voltage reference (via 518) and coupling the test plate (502-504 of figure 5) to a transmitting circuit generating a test signal in response to detecting an input test signal (col. 3, lines 31-47).

As to claim 32, Cilingiroglu discloses in Figs. 1-5, evaluating detected data signal comparing the detected data signal to an expected data signal (col. 3, lines 35-47).

As to claim 44, Cilingiroglu disclose in Figs. 1-5, a test apparatus for an integrated circuit (500 of figure 5, or 110 of figure 1) having plurality of capacitively coupled signal terminals (501 of figure 5) to which a corresponding plurality of receivers are coupled, the receivers generating a respective data signal in response to detecting a respective input data signal (col. 5, lines 30-40), the test apparatus comprising: a test plate (501 of figure 5) to capacitively couple to the signal terminals of the integrated circuit (500 of figure 5); a test transmitter circuit (516, 518 of figure 5) coupled to the test plate (501 of figure 5) to transmit a data signal to at least one of the signal terminals through the test plate (col. 5, lines 30-40); and a test unit (522 of figure 5) coupled to the test signal terminals to evaluate the detected data signal against test criteria (col. 5, lines 30-40).

As to claim 46, Cilingiroglu disclose in Figs. 1-5, the test unit (522 of figure 5) comprising test circuitry to determine the functionality of the receivers coupled to the

signal terminals and the integrity of a capacitor through which the signal terminal is capacitively coupled (col. 5, lines 30-40).

As to claim 47, Cilingiroglu disclose in Figs. 1-5, the test unit comprises test circuitry to compare the detected data signal against an expected data signal (col. 5, lines 30-40);

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cilingiroglu (u.s.p 5,124,660), in view of Vest et al. (u.s.p 6,242,941).

As to claim 26, Cilingiroglu discloses in Figs. 1-5, all of the limitations except for placing the remaining data terminals of the plurality in a high-impedance state. However, Vest et al. disclose in col. 1, lines 63-67, the terminals of the plurality in a high-impedance state for reducing noise in the testing mode. Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Cilingiroglu, and provides the terminals of plurality in high-impedance state, as taught by Vest et al., for reducing noise in the testing mode (col. 1, lines 63, 67).

6. Claims 28, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cilingiroglu (u.s.p 5,124,660), in view of Parker et al. (u.s.p 6,087,842).

As to claim 28, Cilingirolu discloses in Figs. 1-5, all of the limitations except for forming the test plate from a conductive plate layer formed on the semiconductor die. However, Parker et al. disclose in Figs. 6A, forming the test plate (614 of figure 6A) from a conductive plate layer formed on the semiconductor die (600 of figure 6A) for effectively testing the electrical continuity between the paths of integrated circuit (see the abstract). Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the system of Cilingiroglu, and provide the test plate from a conductive plate layer formed on the semiconductor die, as taught by Parker et al, for effectively testing the electrical continuity between the paths of integrated circuit (see the abstract).

As to claim 31, Cilingirolu discloses in Figs. 1-5, the integrated circuit comprising a memory device (110 of figure 1).

7. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cilingiroglu (u.s.p 5,124,660), in view of Seki (u.s.p 6,714,031).

As to claim 45, Cilingiroglu discloses in Figs. 1-5, all of the limitations except for the test transmitter comprising a buffer circuit. However, Seki disclose in Figs. 6, the test transmitter comprising a buffer circuit (61 of figure 6) for delaying in each stage (col. 6, lines 40-45). Therefore, It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify a system of Cilingiroglu, and provide the buffer circuit, as taught by Seki for delaying in each stage (col. 6, lines 40-45).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X. Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN
6/7/05

VINH NGUYEN
PRIMARY EXAMINER
A.U. 2829
06/09/05